of N channel FET forming its emitter, the P well 68 forming its base and N well 67 forming its collector. The transistor 82 is a PNP bipolar transistor with source region 74 of P channel FET forming its emitter, the N well 67 forming its base and the P well 68 forming its collector.

The following are mark-ups to show changes made to paragraph(s) starting at page 13, line 1 and ending at page 14, line 11:

However, applying transient pulses makes it possible to flow a considerably high leakage current in the well. As [prescribed] described in the description of the related art, this leakage current may cause a voltage drop of over 0.6 volts in case of a high resistance between the well contact region and the source of MOS FET. The voltage drop turns on the parasitic bipolar transistors. In the present invention, however, the shunting resistance between emitter and base of the transistor 82 is reduced by forming the first heavily doped region of buried layer 105 at a predetermined portion in the N well region 67 corresponding to the N-well contact region 76. Thus reduced shunting resistance hardly leads to a voltage drop that forces transistor 82 to be turned on, although the leakage current in the N well is considerably high. In other words, the shunting current, a critical current that causes latch-up is higher than the raised leakage current in the N well, which suppresses latch-up. Similarly, the shunting resistance between emitter and base of the transistor 81 can be reduced by forming the second heavily doped region of buried layer 106 at a predetermined portion in the P well region 68 corresponding to the P-well contact region 75. Thus reduced shunting resistance does not result in a voltage drop that causes the

transistor 81 to be turned on, although the leakage current in the P well is considerably high. In other words, the shunting current, a critical current causing latch-up, is higher than the raised leakage current in the P well, thereby preventing latch-up. In the figure, RW is the shunting resistance between emitter and base of the PNP bipolar transistor and RS is the shunting resistance between emitter and base of the NPN bipolar transistor.

The following are mark-ups to show changes made to paragraph(s) starting at page 17, line 6 and ending at page 17, line 18:

Referring to Fig. 3C, a photoresist 102 on the semiconductor substrate 51 including the first N type region [47] 57 injected into the semiconductor substrate 51 is patterned. N type impurities such as P ions are then implanted in the exposed portion to form a second N type region 60. The impurities are injected into the second N type region 60 with a dose of dopants ranging from 3.0 E13 to 1.0 E14 at an acceleration voltage of 200 to 300 KeV. Compared with the impurities injected into the first N type region 57, the ion implantation in the second N type region 60 is performed with more dose of dopants but the acceleration voltage is lowered. Thus the second N type region 60 is located over the first N type region 57.

B. Clean Specification Changes

Please replace paragraph(s) starting at page 12, line 9 and ending at page 12, line 16 with the following paragraph(s):

B1

As shown in Fig. 2, the CMOS semiconductor device 89 includes two parasitic bipolar transistors 81 and 82. The transistor 81 is an NPN bipolar transistor with source region 71 of N channel FET forming its emitter, the P well 68 forming its base and N well 67 forming its collector. The transistor 82 is a PNP bipolar transistor with source region 74 of P channel FET forming its emitter, the N well 67 forming its base and the P well 68 forming its collector.

Please replace paragraph(s) starting at page 13, line 1 and ending at page 14, line 11 with the following paragraph(s):

B2 cont.

However, applying transient pulses makes it possible to flow a considerably high leakage current in the well. As described in the description of the related art, this leakage current may cause a voltage drop of over 0.6 volts in case of a high resistance between the well contact region and the source of MOS FET. The voltage drop turns on the parasitic bipolar transistors. In the present invention, however, the shunting resistance between emitter and base of the transistor 82 is reduced by forming the first heavily doped region of buried layer 105 at a predetermined portion in the N well region 67 corresponding to the N-well contact region 76. Thus reduced shunting resistance hardly leads to a voltage drop that forces transistor 82 to be turned on, although the leakage current in the N well is considerably high. In other words, the shunting

B2 cncl'd

current, a critical current that causes latch-up is higher than the raised leakage current in the N well, which suppresses latch-up. Similarly, the shunting resistance between emitter and base of the transistor 81 can be reduced by forming the second heavily doped region of buried layer 106 at a predetermined portion in the P well region 68 corresponding to the P-well contact region 75. Thus reduced shunting resistance does not result in a voltage drop that causes the transistor 81 to be turned on, although the leakage current in the P well is considerably high. In other words, the shunting current, a critical current causing latch-up, is higher than the raised leakage current in the P well, thereby preventing latch-up. In the figure, RW is the shunting resistance between emitter and base of the PNP bipolar transistor and RS is the shunting resistance between emitter and base of the NPN bipolar transistor.

Please replace paragraph(s) starting at page 17, line 6 and ending at page 17, line 18 with the following paragraph(s):

B3

Referring to Fig. 3C, a photoresist 102 on the semiconductor substrate 51 including the first N type region 57 injected into the semiconductor substrate 51 is patterned. N type impurities such as P ions are then implanted in the exposed portion to form a second N type region 60. The impurities are injected into the second N type region 60 with a dose of dopants ranging from 3.0 E13 to 1.0 E14 at an acceleration voltage of 200 to 300 KeV. Compared with the impurities injected into the first N type region 57, the ion implantation in the second N type

B3 cmd'd

region 60 is performed with more dose of dopants but the acceleration voltage is lowered. Thus the second N type region 60 is located over the first N type region 57.